The invention claimed is:

1. An apparatus for modulating a bit stream onto a pulse signal for transmission, the apparatus comprising:

a pulse generator that generates a selectively delayed and inverted signal pulse responsive to a phase signal and a delay signal;

a phase controller coupled to the pulse generator, the phase controller configured to generate the phase signal responsive to a first data bit of the bit stream; and

a delay controller coupled to the pulse generator, the delay controller configured to generate the delay signal responsive to a second data bit of the bit stream.

2. The apparatus of claim 1, wherein the pulse generator is a monocycle pulse generator and the signal pulse is a monocycle signal pulse generated by the monocycle pulse generator.

3. The apparatus of claim 1, wherein the pulse generator is an Ultra Wideband (UWB) pulse generator and the signal pulse is a UWB signal pulse.

4. The apparatus of claim 1, wherein the signal pulse is selectively delayed by an amount sufficient to substantially decorrelate the delayed signal pulse from a non-delayed signal pulse.

5. The apparatus of claim 4, wherein the delayed signal pulse is orthogonal to the non-delayed signal pulse.

6. The apparatus of claim 1, further comprising:

a time-hopping controller for time-hopping the signal pulse as selectively inverted and delayed.

7. The apparatus of claim 1, wherein the first and second data bits are consecutive bits that are represented by the signal pulse as selectively delayed and inverted.

8. The apparatus of claim 1, wherein the pulse generator comprises:

a first pulse generator that generates a non-inverted signal pulse with no delay;

a second pulse generator that generates a non-inverted signal pulse with a delay;

a third pulse generator that generates an inverted signal pulse with no delay;

a fourth pulse generator that generates an inverted signal pulse with the delay; and

a selector coupled to said first, second, third, and fourth pulse generators, the selector selecting the signal pulse generated by one of the first, second, third, and fourth pulse generators responsive to the phase signal and the delay signal.

9. The apparatus of claim 1, wherein the pulse generator comprises:

a pulse generator that generates a signal pulse, the pulse generator configured to selectively invert the signal pulse responsive to the phase signal and to selectively delay the signal pulse responsive to the delay signal.

10. The apparatus of claim 1, wherein the pulse generator comprises:

a first pulse generator that generates a first pulse;

a second pulse generator that generates a second pulse, the second pulse being inverted with respect to the first pulse;

a selector coupled to the first and second pulse generator, the selector selecting the first pulse generated by the first pulse generator or the second pulse generated by the second pulse generator responsive to the phase signal; and

a delay circuit coupled to the selector, the delay circuit introducing delay to the pulse selected by the selector responsive to the delay signal.

11. A method for modulating a bit stream onto a pulse signal for transmission, the method comprising the steps of:

selectively inverting a signal pulse responsive to a first bit of the bit stream; and

selectively delaying the signal pulse responsive to a second bit of the bit stream.

12. The method of claim 11, wherein the signal pulse is a monocycle signal pulse and wherein the inverting and delaying steps, respectively, comprise the steps of:

selectively inverting the monocycle signal pulse responsive to the first bit of the bit stream; and

selectively delaying the monocycle signal pulse responsive to the second bit of the bit stream.

13. The method of claim 12, wherein the monocycle signal pulse is an Ultra Wideband (UWB) signal pulse.

14. The method of claim 11, wherein the delaying step comprises the step of:

selectively delaying the signal pulse responsive to the second bit of the bit stream by an amount sufficient to substantially decorrelate the delayed signal pulse from the original signal pulse.

15. The method of claim 14, wherein the delaying step comprises the step of:

selectively delaying the signal pulse such that the delayed signal pulse is orthogonal to the signal pulse prior to delay.

16. The method of claim 11, further comprising:

time-hopping the signal pulse as selectively inverted and delayed.

17. The method of claim 11, wherein the inverting step comprises the steps of:

generating a phase signal responsive to the first bit; and

selectively inverting the signal pulse responsive to the phase signal.

18. The method of claim 11, wherein the delaying step comprises the steps of:

generating a delay signal responsive to the second bit; and

selectively delaying the signal pulse responsive to the delay signal.

19. A method for modulating a bit stream onto a pulse signal for transmission, the method comprising the steps of:

receiving a bit stream having a first and a second bit; and

selectively inverting and delaying a signal pulse responsive to the first and second bits of the bit stream.

20. The method of claim 19, wherein the inverting and delaying step comprises the steps of:

generating a phase signal and a delay signal responsive the first and second bits of the bit stream; and

selectively inverting and delaying the signal pulse responsive to the phase signal and the delay signal.

21. The method of claim 19, wherein the inverting and delaying step comprises the steps of:

generating a non-inverted signal pulse with no delay, a non-inverted signal pulse with delay, an inverted signal pulse without delay, and an inverted signal pulse with delay; and

selecting one of the generated signal pulses responsive to the first and second bits of the bit stream.

22. The method of claim 21, wherein the selecting step comprises the steps of:

generating a phase signal and a delay signal responsive the first and second bits; and

selecting one of the generated signal pulses responsive to the phase signal and the delay signal.

23. The method of claim 19, wherein the inverting and delaying step comprises the steps of:

generating a non-inverted signal pulse and an inverted signal pulse;

selecting one of the generated signal pulses responsive to the first bit of the bit stream; and

selectively delaying the selected one of the generated signal pulses responsive to the second bit of the bit stream.

24. A system for modulating a bit stream onto a pulse signal for transmission, the system comprising:

means for selectively inverting a signal pulse responsive to a first bit of the bit stream; and

means for selectively delaying the signal pulse responsive to a second bit of the bit stream.

25. The system of claim 24, further comprising:

means for time-hopping the signal pulse as selectively inverted and delayed.

26. The system of claim 24, wherein the inverting means comprises:

means for generating a phase signal responsive to the first bit; and

means for selectively inverting the signal pulse responsive to the phase signal.

27. The system of claim 24, wherein the delaying means comprises:

means for generating a delay signal responsive to the second bit; and

means for selectively delaying the signal pulse responsive to the delay signal.

28. A computer readable carrier including software that is configured to control a computer to implement a modulation method embodied in a computer readable medium, the modulation method including the steps of:

selectively inverting a signal pulse responsive to a first bit of the bit stream; and

selectively delaying the signal pulse responsive to a second bit of the bit stream.

29. The computer readable carrier of claim 28, wherein the inverting step for implementation by the computer comprises the steps of:

generating a phase signal responsive to the first bit; and

selectively inverting the signal pulse responsive to the phase signal.

30. The computer readable carrier of claim 28, wherein the delaying step for implementation by the computer comprises the steps of:

generating a delay signal responsive to the second bit; and

selectively delaying the signal pulse responsive to the delay signal.

31. The computer readable carrier of claim 28, wherein the method implemented by the general purpose computer further includes the step of:

time-hopping the selectively inverted and delayed signal pulse.